Novel Full-chip Verification Methodologies for Domain-crossing and Transient Latch-up Damage Prevention

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Biography

- When Mr. David Klein received a M.S. degree in Electrical Engineering from Washington State University in 1995, he never intended to get into ESD research and design. He joined Integrated Device Technology as a mixed signal engineer, but the first project he was assigned to failed during HBM testing. After getting that project sorted out, he slowly became the ESD resource for his design center during his spare time, consulting on ESD strategy, design and implementation. In 2007, his spare time ran out, so he switched to doing ESD full time. After nearly 16 years at IDT and two and half years at Freescale, David currently enjoys the challenges of providing ESD solutions to human interface ASICs as a senior ESD manager at Synaptics. Along the way he's been awarded a few patents and managed to collaborate on a paper or two.

Abstract

As technologies shrink resulting in lower junction and oxide breakdown voltage levels, internal circuits become more susceptible to damage from IEC-61000-4-2 system level stress. This internal damage can result from oxide break down or transient latch-up triggered by the IEC stress. Two analysis tools are presented which help to find weak points in resistive supply and signal paths and locate ineffective guard rings due to interconnect resistance.

Due to resistive isolation of the ground nets between driver and receiver (D/R) pairs, the most common damage observed is to domain crossing signal receivers. However, damage can also occur on receivers where the D/R pair are on the same ground net. Using a tool created for CDM analysis [1], the resistance between D/R pairs is analyzed at the full chip level for IEC-61000-4-2 failure prevention. The proposed methodology is capable of finding D/R weak spots prior to tape out.

Ineffective guard rings also cause latch-up and catastrophic damage in ASICs. To find these weak guard rings, a guard ring simulator is used to calculate the resistance map (Rmap) of each guard ring to its power pad(s). This approach is demonstrated to be very useful for finding potentially ineffective guard rings.

CDM Analysis Tool

- Why use a CDM tool to analyze IEC-induced failure?
  - IEC pulse has two peaks. The 1st peak has a very fast rise time and high current level as shown in Figure 1

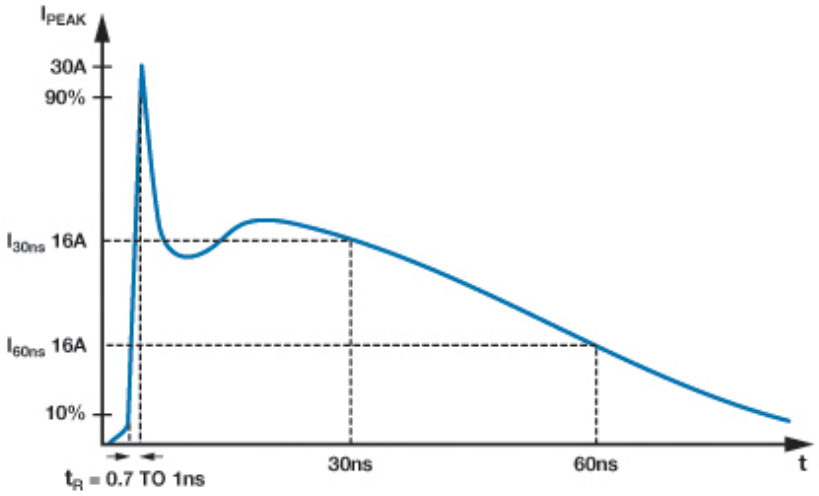


Figure 1. Ideal 8kV IEC-61000-4-2 waveform.

  - The first peak's electrical characteristics are very similar to a CDM pulse

CDM Analysis Tool

- Why use a CDM tool to analyze IEC-induced failure? (cont.)
  - Due to high displacement current levels, the 1st peak in IEC pulse is usually the cause of damage to internal circuits like level shifters and driver/receiver (D/R) pairs
  - Our test case passed 1kV CDM but failed 8kV IEC contact discharge. Because the damage was internal gate oxide damage, it looked like CDM damage
  - High ground resistance without local secondary ESD protection is the typical reason for such damage
  - The tool can highlight devices with high risk of damage during CDM and IEC test
  - Simple setup and fast simulation

CDM Analysis Tool

- Introduction of CDM Analysis Tool
  - DC simulation
  - Runs on the full chip level
  - Calculates and lists ground path resistance for every driver/receiver (D/R) pair
  - Similar to a FDCDM test, it simulates discharge on each package pin
  - Gate oxide damage is more common for receivers of domain crossing signals. However, as shown in Figure 2, during an ESD event, even devices sharing the same supplies can be damaged. The tool identifies receiving devices at risk for both domain crossing and intra-domain D/R pairs

CDM Analysis Tool

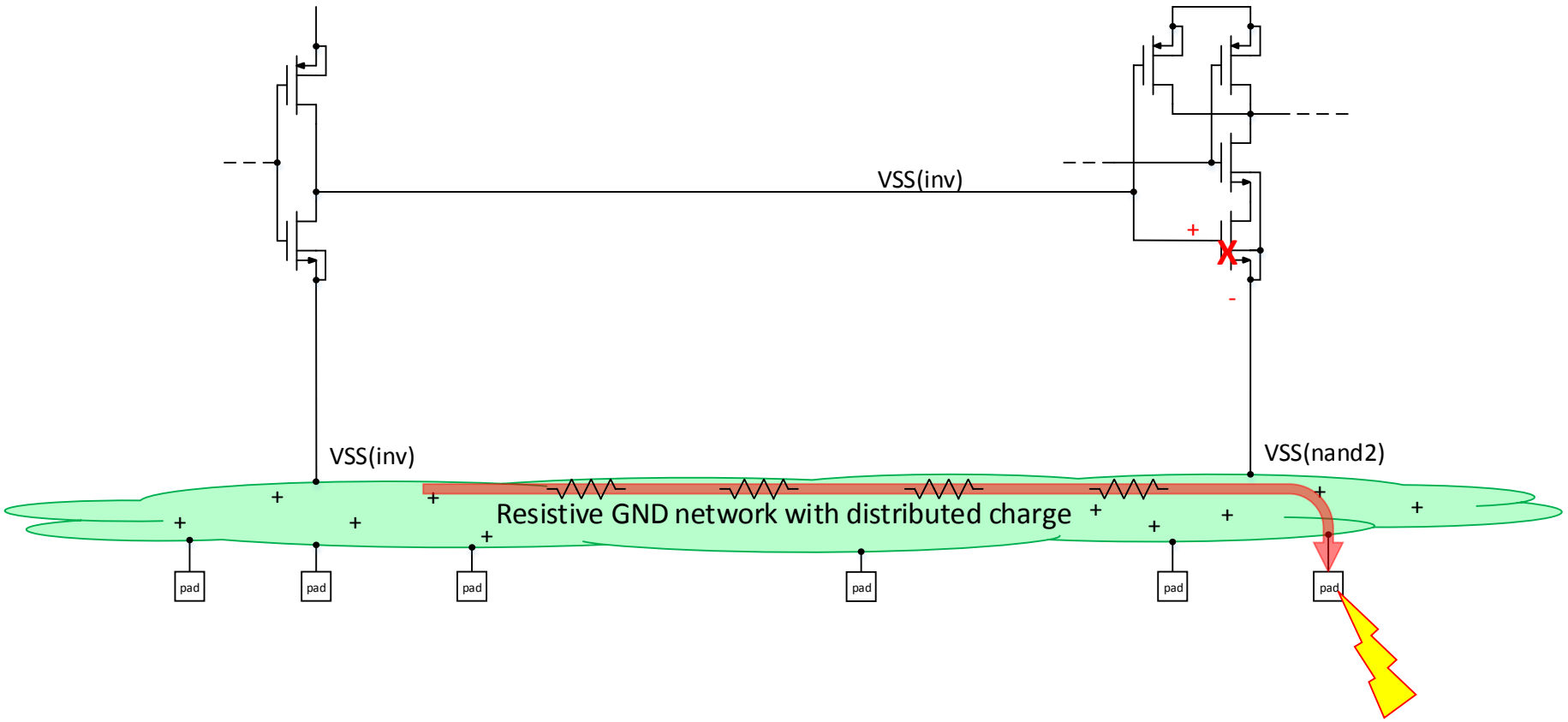


Figure 2. Conceptual illustration of a D/R pair. The bottom NMOS in the NAND2 will have the voltage across its gate oxide, V_{GS}, determined by the current through the resistive GND network. If $V_{SS(inv)} – VSS_{(nand2)}$ is larger than the oxide breakdown voltage, V_{BDOX}, this NMOS is at risk during CDM and IEC testing.

CDM Analysis Tool

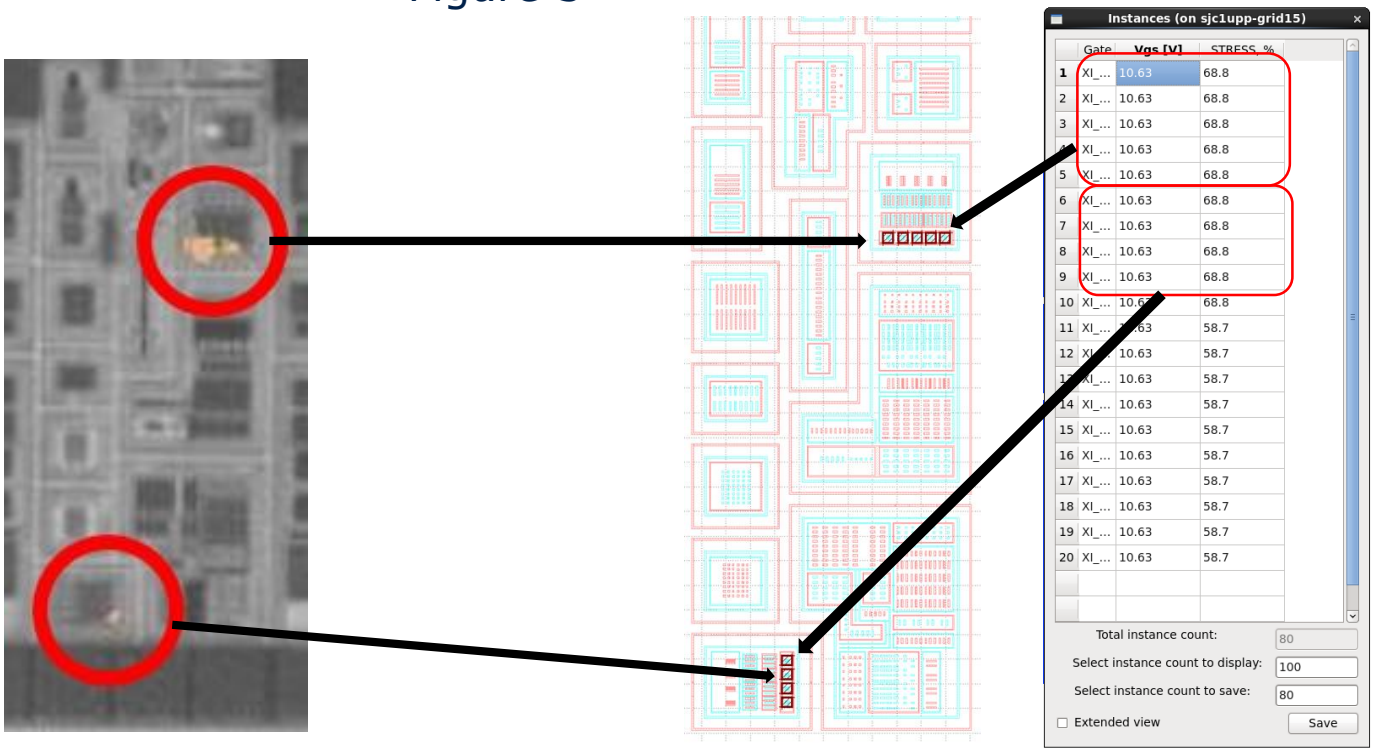
- Charge distribution mechanism
  - Charge is induced equally over the chip on the metals or guard ring.
  - Wire-bond/COG packages have charge distributed on upper level metals
  - Flip-chip packages have charges distributed on substrate contacts (guard rings)
  - The area of the metals or guard ring determine the amount of charge
- The simulation database includes:
  - LVS database generated from a physical verification tool
  - Regular ESRA pin/pad definition files
  - Stress check with V_{GS} breakdown voltages of the transistors used in the design
  - Models for ESD devices (diodes, triggered clamps, snapback clamps, thyristors)
  - Technology files

Study Case of CDM simulation

- Failure Case
  - Failure only occurred during IEC-61000-4-2 contact discharge to the ground plane of the fPCB that was part of a face down display module. The damage was to the integrated touch and display driver ASIC which was fully operational during the test
  - ASIC level FDCDM testing did not replicate the failure
  - Abnormal photoemission is shown in Figure 3 along with analysis results
- Failure investigation using the CDM analysis tool
  - Simulation current is set to 10A
  - Figure 4 lists the overstress D/R pairs in the suspicious region
  - The “STRESS, %” is the percentage of overstress. For example, “68.8%” means the V_{GS} on receiver is 1.688 higher than the breakdown voltage V_{BDOX}

Study Case of CDM simulation

Figure 3



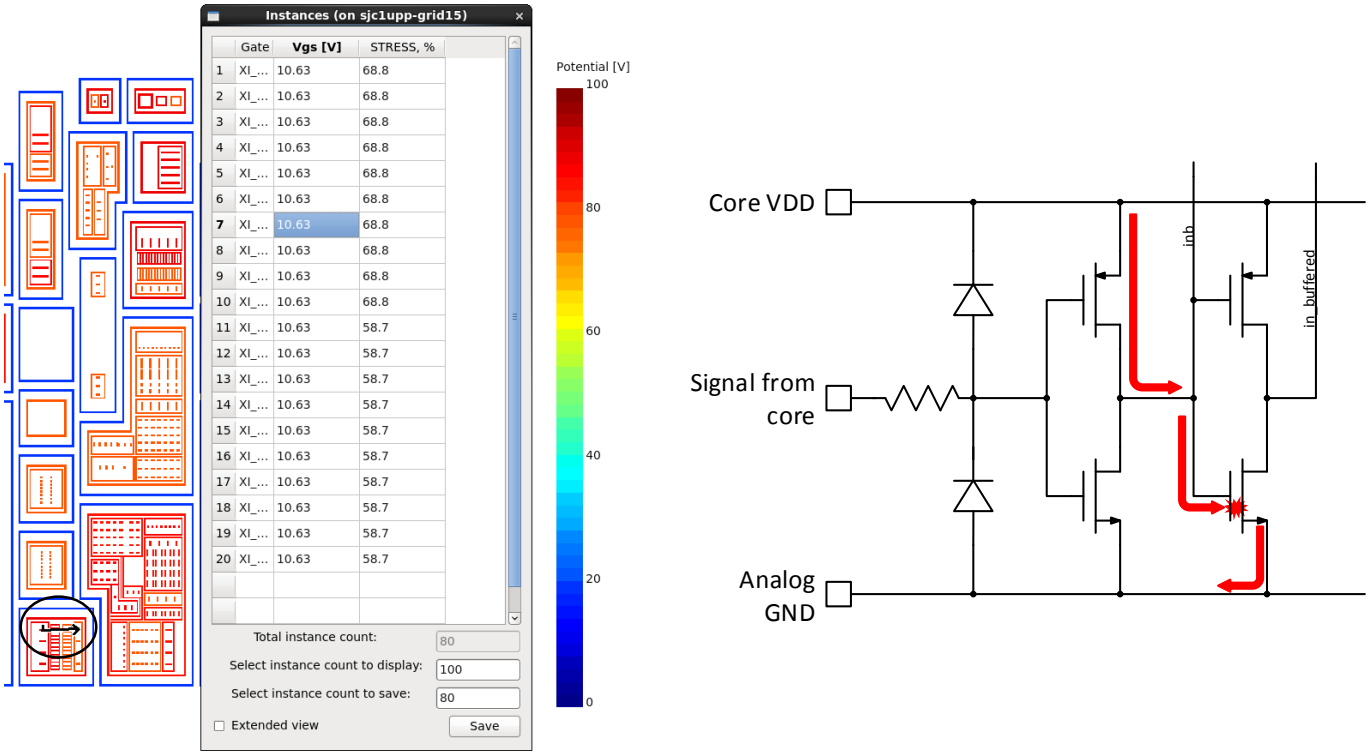
Left: Photoemission at the failure locations in the receivers. During this capture, the ASIC is powered up and operational with only the functionality of this block compromised.

Please note: After IEC stress, a random distribution of the devices in the circled areas would be damaged

Right: The D/R pairs found by the tool to be at risk

Study Case of CDM simulation

Figure 4.



Left: List of overstressed D/R pairs. The circled black arrow highlights the path from driver to receiver.

Right: The schematic with discharge path of the D/R pair

Study Case of CDM simulation

- Analysis and Improvement
  - In this design, the driver and receiver use the same analog ground. There is relatively high resistance between the core ground and the analog ground at this location allowing for large core V_{DD} to analog ground voltage buildup.
  - Inspection of the layout showed no nearby anti-parallel diodes between the core and analog ground nets
  - Anti-parallel diodes were added between these two grounds near the at-risk NMOS as shown in Figure 5
    - After these diodes were added, simulation no longer shows overstress in this region
    - The new silicon passed the IEC-61000-4-2 test

Study Case of CDM simulation

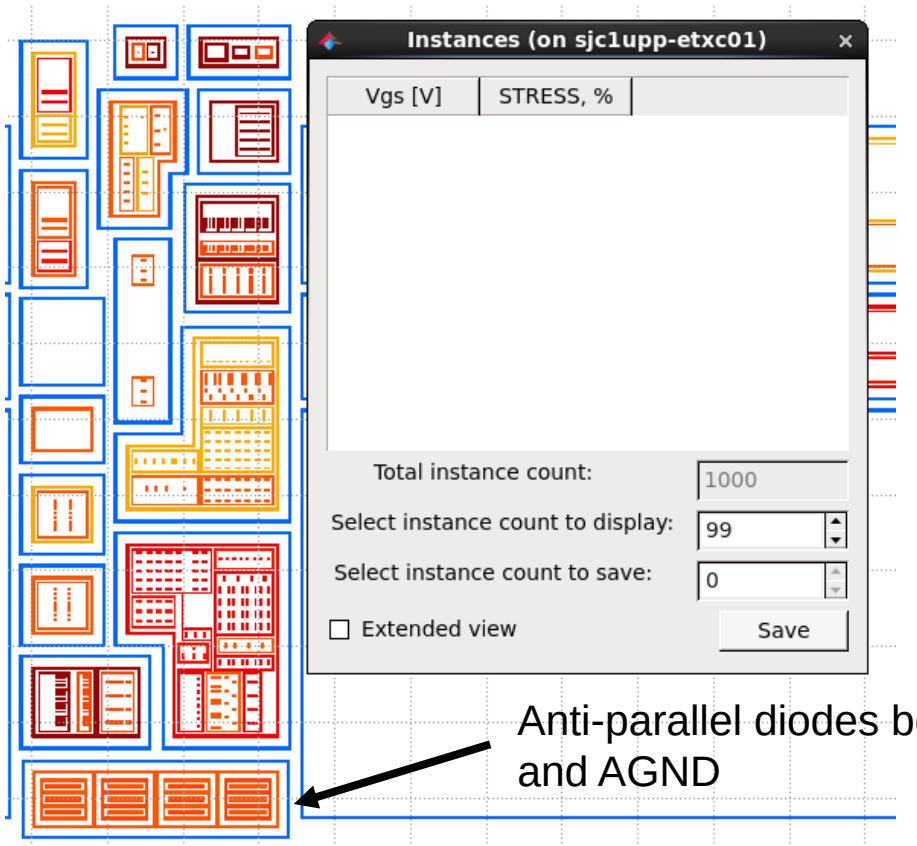


Figure 5. Simulation results with the fix (adding new anti-parallel diode)

Guard Ring Analysis Tool

- Introduction of Guard Ring Analysis Tool
  - DC simulation
  - Generates Rmap from each power pad to its guard rings
  - Calculates the resistance from a user defined sampling resolution on the guard ring to its corresponding power pad. For example,

    p2p_rmap_multinets net_pattern=AGND layer=metal7 dxy=1 -o ${runname}_AGND

    dxy=1 defines a sample point every 1μm in both the X and Y dimensions over each guard ring
  - As shown in Figure 6, there are eight sample points (A-H) on the guard ring
  - Output is a graphical heat map for each supply and a text file with tables of the location of the highest resistance per layer for each supply
- The simulation database includes:
  - LVS database generated from a physical verification tool
  - Regular ESRA pin/pad definition files
  - Technology files

Study Case of Guard Ring simulation

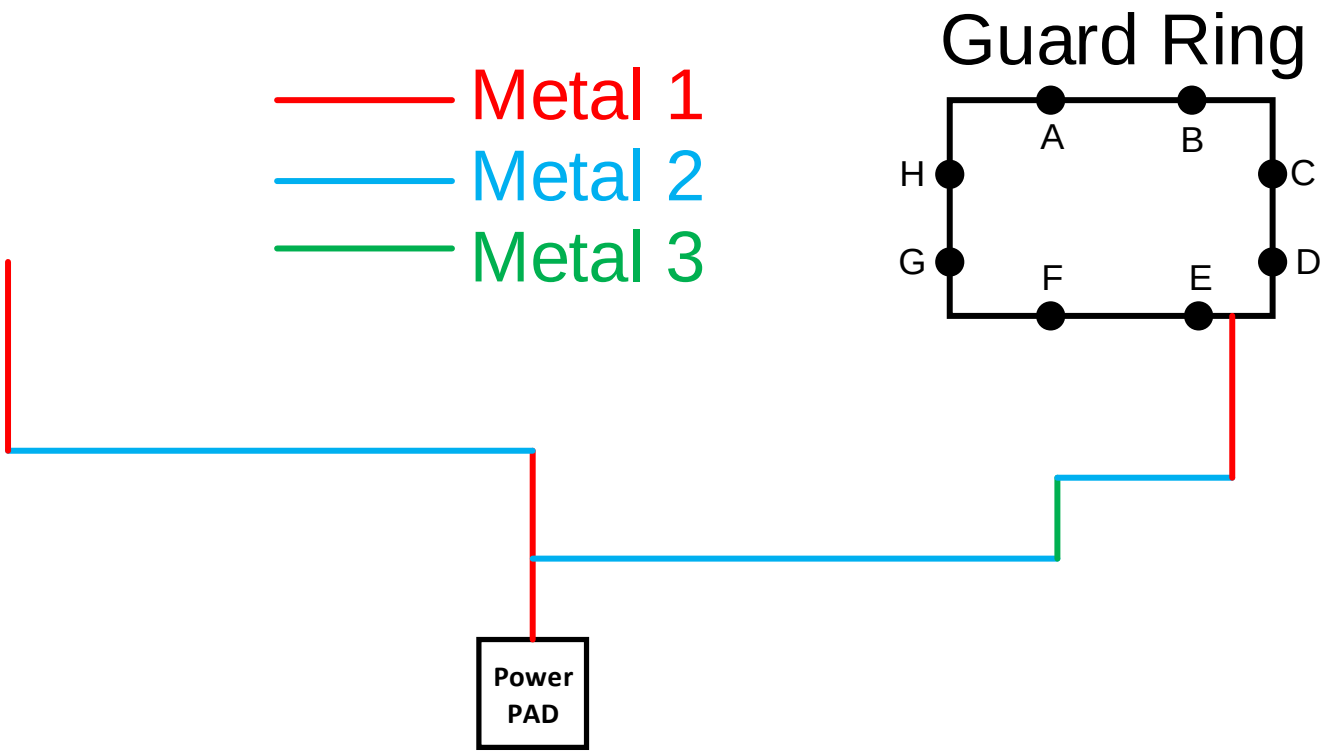


Figure 6. Conceptual illustration of the guard ring analysis. The tool calculates the resistance from each sample point (A-H) to the power pads.

Study Case of Guard Ring simulation

- Failure Case
  - During IEC-61000-4-2 contact discharge to the ground plane of an fPCB that was part of a face down display module, damage occurred to an internal circuit that had been used in multiple earlier designs without issue. The damage looked like latch-up.
  - ASIC level FDCDM and latch-up testing did not replicate the failure
  - Analysis of the ESD network for the block in question did not raise any red flags
  - As shown in Figures 7 and 8, guard ring analysis found guard rings with resistances in excess of 13.8kΩ (VSP) and 12.6kΩ (AGND) adjacent to the failure location
  - A three metal mask change reduced the resistance to less than 10Ω on the AGND guard ring and less than 320Ω on the VDD guard ring and fixed the problem

Study Case of Guard Ring simulation

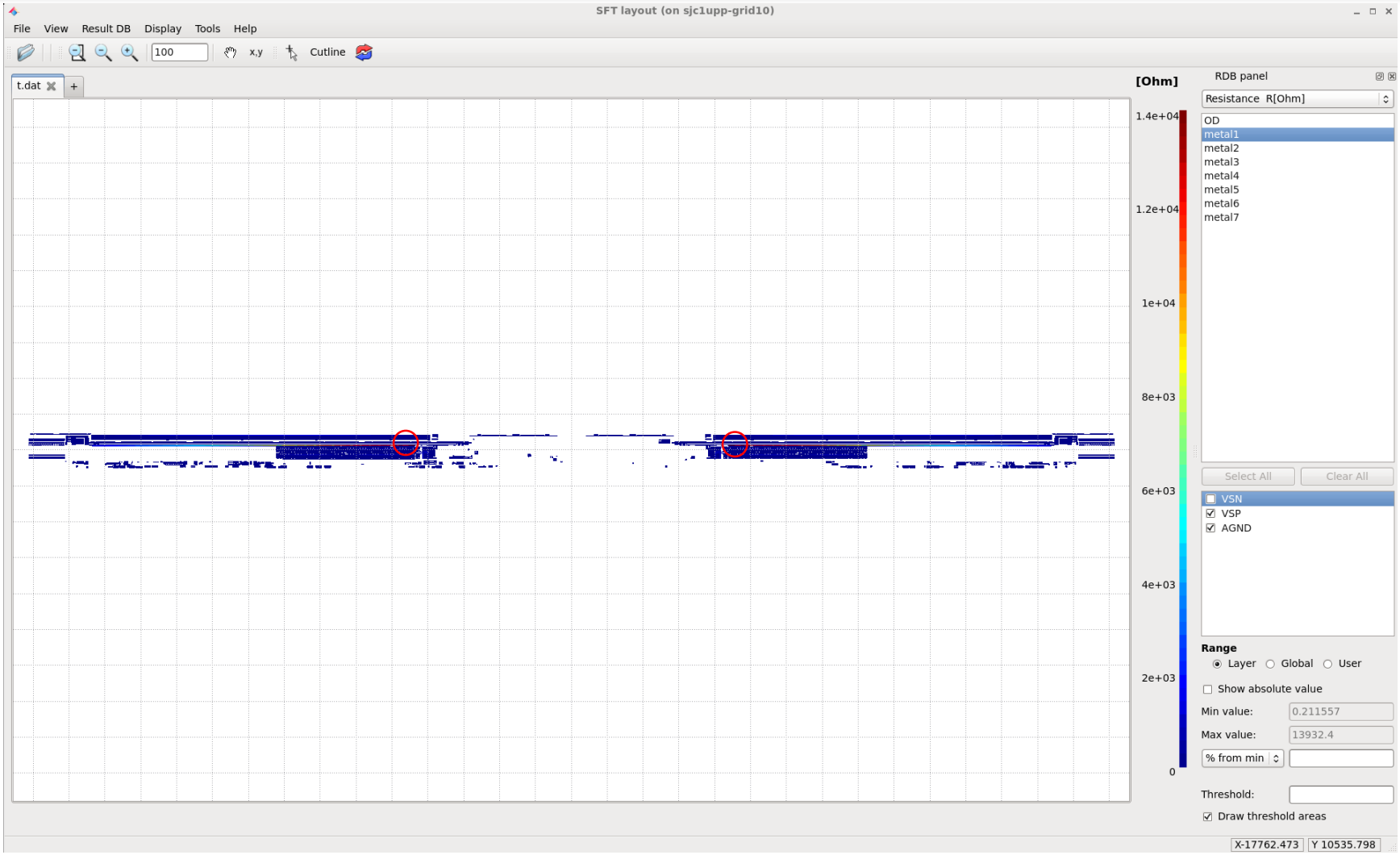


Figure 7. Rmap of AGND and VSP supply networks along with damage locations in red circles

Study Case of Guard Ring simulation

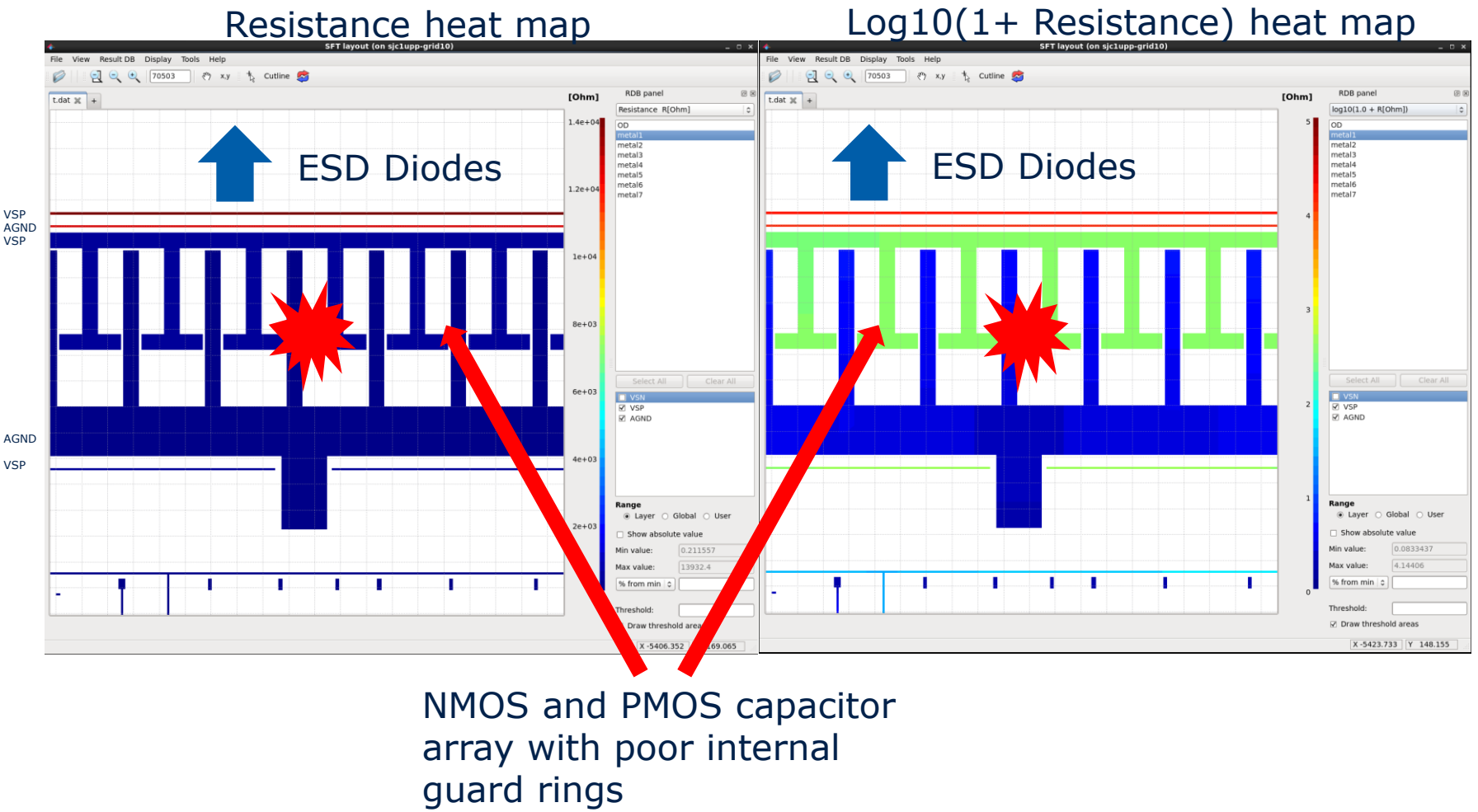


Figure 8. Zoomed in and annotated screen shots of Rmap for AGND and VSP supply networks next to damage location

Conclusion

In this presentation, we successfully used the CDM analysis tool from SFT to assist in debugging IEC induced failures in D/R pairs. The tool is capable of highlighting high ground resistance in the D/R pairs and the results match the failure analysis results. This makes the tool very useful for analyzing the full-chip design to find at-risk D/R pairs. It also allows ASIC evaluation and prediction of IEC performance.

We also used the guard ring analysis tool from SFT to check for high guard ring resistance from the power pads. It found weak connectivity to guard-rings resulting in transient induced latch-up. This tool can easily identify weak guard ring connectivity, providing guidance to layout for guard ring interconnect improvement which should result in improved latch-up immunity and noise isolation.

References

[1] Melanie Etherton, Scott Ruth, James W. Miller, et al, "*A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures*," 2015 ESD Symposium, Reno, NV, USA.